

WHAT IS CLAIMED IS:

1. A CDMA transmitter comprising:

a first baseband combiner capable of receiving N baseband chip streams, each of said N baseband chip streams comprising a sequence of chips, each chip having one of a positive amplitude value and a negative amplitude value, wherein said first baseband combiner combines chips from corresponding time slots in each of said N baseband chip streams to thereby generate a first composite baseband chip sequence;

a data processor coupled to said first baseband combiner capable of detecting a first peak amplitude in said first composite baseband chip sequence that exceeds a pre-determined maximum threshold and determining an amplitude and a polarity of a first compensation pulse associated with said first peak amplitude; and

a pulse generator coupled to said data processor capable of generating said first compensation pulse having said amplitude and said polarity determined by said data processor, wherein said first baseband combiner receives said first compensation pulse and combines said first compensation pulse with said first composite baseband chip sequence during a chip time slot corresponding to said first peak amplitude.

1 2. The CDMA transmitter as set forth in Claim 1 wherein said
2 data processor determines said amplitude and said polarity of said
3 first compensation pulse as a function of a maximum peak-to-average
4 power ratio associated with said first composite baseband chip
5 sequence.

3. The CDMA transmitter as set forth in Claim 2 wherein said
each chip in each of said N baseband chip streams has one of a +1
relative amplitude value and -1 relative amplitude value.

4. The CDMA transmitter as set forth in Claim 3 wherein said
CDMA transmitter is a quadrature phase-shift keying (QPSK)
transmitter and said first composite baseband chip sequence is a
composite in-phase chip sequence.

1 5. The CDMA transmitter as set forth in Claim 1 further
2 comprising:

3 a second baseband combiner capable of receiving M
4 baseband chip streams, each of said M baseband chip streams
5 comprising a sequence of chips, each chip having one of a positive
6 amplitude value and a negative amplitude value, wherein said second
7 baseband combiner combines chips from corresponding time slots in
8 each of said M baseband chip streams to thereby generate a second
9 composite baseband chip sequence, wherein said data processor is
10 coupled to said second baseband combiner and is further capable of
11 detecting a second peak amplitude in said second composite baseband
12 chip sequence that exceeds a pre-determined maximum threshold and
13 determining an amplitude and a polarity of a second compensation
14 pulse associated with said second peak amplitude; and

15 a second pulse generator coupled to said data processor
16 capable of generating said second compensation pulse having said
17 amplitude and said polarity determined by said data processor,
18 wherein said second baseband combiner receives said second
19 compensation pulse and combines said second compensation pulse with
20 said second composite baseband chip sequence during a chip time
21 slot corresponding to said second peak amplitude.

1 6. The CDMA transmitter as set forth in Claim 5 wherein said
2 data processor determines said amplitude and said polarity of said
3 second compensation pulse as a function of a maximum peak-to-
4 average power ratio associated with said second composite baseband
5 chip sequence.

7. The CDMA transmitter as set forth in Claim 6 wherein said
each chip in each of said M baseband chip streams has one of a +1
relative amplitude value and -1 relative amplitude value.

8. The CDMA transmitter as set forth in Claim 7 wherein said
CDMA transmitter is a quadrature phase-shift keying (QPSK)
transmitter and said second composite baseband chip sequence is a
composite quadrature chip sequence.

1 9. A wireless communication network comprising:

2 a plurality of base stations capable of communicating
3 with a plurality of mobile stations disposed in a coverage area of
4 said plurality of base stations; and

5 a CDMA transmitter associated with at least one of said
6 plurality of base stations, said CDMA transmitter comprising:

7 a first baseband combiner capable of receiving N
8 baseband chip streams, each of said N baseband chip streams
9 comprising a sequence of chips, each chip having one of a
10 positive amplitude value and a negative amplitude value,
11 wherein said first baseband combiner combines chips from
12 corresponding time slots in each of said N baseband chip
13 streams to thereby generate a first composite baseband chip
14 sequence;

15 a data processor coupled to said first baseband
16 combiner capable of detecting a first peak amplitude in said
17 first composite baseband chip sequence that exceeds a pre-
18 determined maximum threshold and determining an amplitude and
19 a polarity of a first compensation pulse associated with said
20 first peak amplitude; and

21 a pulse generator coupled to said data processor
22 capable of generating said first compensation pulse having

23 said amplitude and said polarity determined by said data
24 processor, wherein said first baseband combiner receives said
25 first compensation pulse and combines said first compensation
26 pulse with said first composite baseband chip sequence during
27 a chip time slot corresponding to said first peak amplitude.

10. The wireless communication network as set forth in
Claim 9 wherein said data processor determines said amplitude and
said polarity of said first compensation pulse as a function of a
maximum peak-to-average power ratio associated with said first
composite baseband chip sequence.

11. The wireless communication network as set forth in
Claim 10 wherein said each chip in each of said N baseband chip
streams has one of a +1 relative amplitude value and -1 relative
amplitude value.

1 12. The wireless communication network as set forth in
2 Claim 11 wherein said CDMA transmitter is a quadrature phase-shift
3 keying (QPSK) transmitter and said first composite baseband chip
4 sequence is a composite in-phase chip sequence.

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1 13. The wireless communication network as set forth in
2 Claim 7, wherein the CDMA transmitter further comprises:

3 a second baseband combiner capable of receiving M
4 baseband chip streams, each of said M baseband chip streams
5 comprising a sequence of chips, each chip having one of a positive
6 amplitude value and a negative amplitude value, wherein said second
7 baseband combiner combines chips from corresponding time slots in
8 each of said M baseband chip streams to thereby generate a second
9 composite baseband chip sequence, wherein said data processor is
10 coupled to said second baseband combiner and is further capable of
11 detecting a second peak amplitude in said second composite baseband
12 chip sequence that exceeds a pre-determined maximum threshold and
13 determining an amplitude and a polarity of a second compensation
14 pulse associated with said second peak amplitude; and

15 a second pulse generator coupled to said data processor
16 capable of generating said second compensation pulse having said
17 amplitude and said polarity determined by said data processor,
18 wherein said second baseband combiner receives said second
19 compensation pulse and combines said second compensation pulse with
20 said second composite baseband chip sequence during a chip time
21 slot corresponding to said second peak amplitude.

1 14. The wireless communication network as set forth in
2 Claim 13 wherein said data processor determines said amplitude and
3 said polarity of said second compensation pulse as a function of a
4 maximum peak-to-average power ratio associated with said second
5 composite baseband chip sequence.

15. The wireless communication network as set forth in
Claim 14 wherein said each chip in each of said M baseband chip
streams has one of a +1 relative amplitude value and -1 relative
amplitude value.

16. The wireless communication network as set forth in
Claim 15 wherein said CDMA transmitter is a quadrature phase-shift
keying (QPSK) transmitter and said second composite baseband chip
sequence is a composite quadrature chip sequence.

1 17. A method of processing baseband chip streams in a CDMA
2 transmitter, the method comprising the steps of:

3 receiving N baseband chip streams, each of the N baseband
4 chip streams comprising a sequence of chips, each chip having one
5 of a positive amplitude value and a negative amplitude value;

6 combining chips from corresponding time slots in each of
7 the N baseband chip streams to thereby generate a first composite
8 baseband chip sequence;

9 detecting a first peak amplitude in the first composite
10 baseband chip sequence that exceeds a pre-determined maximum
11 threshold;

12 determining an amplitude and a polarity of a first
13 compensation pulse associated with the first peak amplitude;

14 generating the first compensation pulse having the
15 determined amplitude and polarity; and

16 combining the first compensation pulse with the first
17 composite baseband chip sequence during a chip time slot
18 corresponding to the first peak amplitude.

1 18. The method as set forth in Claim 17 wherein the amplitude
2 and the polarity of the first compensation pulse are determined as
3 a function of a maximum peak-to-average power ratio associated with
4 the first composite baseband chip sequence.

1 19. The method as set forth in Claim 18 wherein each chip in
each of the N baseband chip streams has one of a +1 relative
amplitude value and -1 relative amplitude value.

1 20. The method as set forth in Claim 17 further comprising
2 the steps of:

3 receiving M baseband chip streams, each of the M baseband
4 chip streams comprising a sequence of chips, each chip having one
5 of a positive amplitude value and a negative amplitude value;

6 combining chips from corresponding time slots in each of
7 the M baseband chip streams to thereby generate a second composite
8 baseband chip sequence;

9 detecting a second peak amplitude in the second composite
10 baseband chip sequence that exceeds a pre-determined maximum
11 threshold;

12 determining an amplitude and a polarity of a second
13 compensation pulse associated with the second peak amplitude;

14 generating the second compensation pulse having the
15 determined amplitude and polarity; and

16 combining the second compensation pulse with the second
17 composite baseband chip sequence during a chip time slot
18 corresponding to the second peak amplitude.

1 21. The method as set forth in Claim 20 wherein the amplitude
2 and the polarity of the second compensation pulse are determined as
3 a function of a maximum peak-to-average power ratio associated with
4 the second composite baseband chip sequence.

1 22. The method as set forth in Claim 21 wherein each chip in
each of the M baseband chip streams has one of a +1 relative
amplitude value and -1 relative amplitude value.